ECE 5362 (Proposed): Computer Architecture and Design

Course Description

Design of general purpose digital computers including arithmetic and control units, input/output, and memory subsystems.

Prior Course Number: 662
Transcript Abbreviation: Cmptr Arch/Design
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Undergrad, Graduate
Student Ranks: Junior, Senior, Masters, Doctoral
Course Offerings: Autumn, Spring
Flex Scheduled Course: Never
Course Frequency: Every Year
Course Length: 14 Week
Credits: 3.0
Repeatable: No
Time Distribution: 3.0 hr Lec
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: Prereq: 2560 (265) and 3561 (561), and undergraduate enrollment in ECE, CSE, or EngPhysics major; or Grad standing in Engineering.
Exclusions: Not open to students with credit for 662, CSE 675.01, or 675.02.
Cross-Listings:

Course Rationale: Existing course.

The course is required for this unit's degrees, majors, and/or minors: Yes
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code: 14.0902
Subsidy Level: Doctoral Course

Programs

Abbreviation	Description
CpE	Computer Engineering
EE	Electrical Engineering

Course Goals

Be competent with typical assembly/machine instructions, as well as the key architecture design principles such as RISC vs. CISC.
Master designing control unit systems to meet the requirements of the instruction set given the computer registers and hardware
Be competent with CPU control design tools
Master memory/cache system design algorithms such as cache mapping and replacement

Be familiar with advanced architectural features such as pipelining, fast adder, and fast multiplication
Be exposed to embedded systems

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Design of computer registers, buses, and control lines with timing considerations	5.0							
Instruction sets and their implementation in register transfers	6.0							
Hardwired and microprogrammed control units	4.0							
Simulation of control units using software to verify correctness of control unit design	4.0							
Memory units including cache memory	5.0							
Input/Output systems including polling, interrupt and DMA	3.0							
Fast multiplication and floating point operations	5.0							
Basic processing unit and pipelining	5.0							
Embedded systems	1.0							

Representative Assignments

Design the register transfers to implement a set of instructions on paper.
Use a simulator to design the complete control unit specifications for a complete instruction set given the hardware paths.
Manually execute a given assembly/machine program to derive the contents of registers and memory.
Apply cache mapping and replacement algorithms to determine the cache contents of a given program.

Grades

Aspect	Percent
Homework	14%
Computer problems	16%
Midterm Exams	40%
Final Exam	30%

Representative Textbooks and Other Course Materials

Title	Author
Computer Organization and Embedded Systems	Hamacher, Vranesic, Zaky and Manjikian

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
***	a	An ability to apply knowledge of mathematics, science, and engineering.
	b	An ability to design and conduct experiments, as well as to analyze and interpret data.
***	c	An ability to design a system, component, or process to meet desired needs.
	d	An ability to function on multi-disciplinary teams.
	e	An ability to identify, formulate, and solve engineering problems.
	f	An understanding of professional and ethical responsibility.

Course Contribution		College Outcome
	g	An ability to communicate effectively.
	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
	i	A recognition of the need for, and an ability to engage in life-long learning.
	j	A knowledge of contemporary issues.
***	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Additional Notes or Comments

Update course title, abbreviation, prereqs, exclusions, goals, and topic to match university format.

UPdate prereqs to clarify which course are CSE; entered in Curriculum.OSU today also. 4/5/12
Change 3367 to 3561 in prereqs may 7, 2012

Add "and undegraduate enrollment in ECE, CSE, or EngPhysics major" to aprallel other core courses 2/13/13.

Change offering to both semesters, is a required course. Checke "required course box.3/31/13

Updated text version. 10/30/14 ced.

Add "grad standing in engineering" to prereqs. Update goals, topics, assignments, grading. 6/17/16 BLA

edited text info, 5/10/17, CED

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