ECE 5037 (Proposed): Solid State Microelectronics Laboratory

Course Description

Introduction to laboratory techniques for semiconductor device fabrication including oxidation, chemical processes, photolithography, diffusion, and metalization; fabrication and measurements of planar diodes and transistors.

Prior Course Number: 637
Transcript Abbreviation: Sld St Micro Lab
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Undergrad, Graduate
Student Ranks: Junior, Senior, Masters, Doctoral
Course Offerings: Autumn
Flex Scheduled Course: Never
Course Frequency: Every Year
Course Length: 14 Week
Credits: 4.0
Repeatable: No
Time Distribution: 2.0 hr Lec, 4.0 hr Lab
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: Prereq or concur: 3030 (432), and acceptance in ECE, MSE or EngPhysics major; or Grad standing in Engineering, Biological Sciences, or Math and Physical Sciences.
Exclusions: Not open to students with credit for 637.
Cross-Listings:

Course Rationale: Existing course.

The course is required for this unit's degrees, majors, and/or minors: No
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code: 14.1001
Subsidy Level: Doctoral Course

Programs

Abbreviation	Description
CpE	Computer Engineering
EE	Electrical Engineering

Course Goals

Be competent with the basic techniques for fabrication of integrated circuits
Be competent with computer tools for simulation of integrated circuit fabrication processes
Be competent in applying knowledge learned in prerequisite semiconductor devices courses to fabrication of MOS transistors, other semiconductor devices, and test structures

Be competent in performing current-voltage and capacitance-voltage characterization of semiconductor devices and test structures fabricated in lab
Be competent in extraction of device parameters from and analysis and interpretation of test results
Be familiar with cleanroom procedures, and with safe use of the hazardous materials and equipment used in semiconductor device fabrication

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Lab safety, overview of class MOS process	1.0							
Sheet resistance, four-point probe, wafer cleaning	2.0							
Oxidation of silicon - Deal-Grove model, technology, process design	3.0							
Process simulation - oxidation and diffusion, extraction of parameters from simulation results, basic models	4.0							
Diffusion - technology, macroscopic solutions of diffusion equation, microscopic mechanisms, process design	3.0							
Photolithography; photomask alignment, tolerances and layout; etching	3.0							
Gate dielectrics	1.0							
Device testing - MOS C-V/BTS & TLM contact resistance	2.0							
Ion implantation	2.0							
Process simulation - ion implantation, deposition, etching	3.0							
Metal contact deposition - evaporation and sputter deposition	2.0							
Overview of a CMOS process	1.0							
Introduction to working in a cleanroom, initial silicon wafer characterization, wafer cleaning			4.5					
Oxidation of silicon wafers: field oxidation and gate oxidation			9.0					
Diffusion of dopant impurities into silicon wafers			9.0					
Photolithography processes to mask diffusion regions and gate regions, and to define contact vias and metal patterns on the silicon wafers			18.0					
Metal deposition onto the silicon wafers			4.5					
Demonstration of use of test equipment			4.0					
Current-voltage characterization of fabricated devices and test structures			8.0					
Capacitance-voltage characterization of fabricated test structures			2.0					

Representative Assignments

Weekly pre-lab assignments that are predictive of outcomes to expect for that lab session and include process simulation work.
Weekly post-lab assignments that analyze results of measurements and observation in lab, with comparison to pre-lab expectations.
Process simulation assignments.
A formal final report on the results of device characterization.
Several homework assignments on the theory underlying the processes and measurements being performed in lab, and design of unit processes such as oxidation and diffusion.

Grades

Aspect	Percent
Homework	15%
Midterm Exam	15%
Final Exam	20%
Device Testing Lab Report	15%
Lab Rules and Participation	10%
Pre-lab Assignments	10%
Post-Lab Assignments	10%
Process Simulation Assignments	5%

Representative Textbooks and Other Course Materials

Title	Author
Fabrication Engineering at the Micro- and Nanoscale	Campbell, S.A.

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
***	a	An ability to apply knowledge of mathematics, science, and engineering.
***	b	An ability to design and conduct experiments, as well as to analyze and interpret data.
**	c	An ability to design a system, component, or process to meet desired needs.
	d	An ability to function on multi-disciplinary teams.
**	e	An ability to identify, formulate, and solve engineering problems.
*	f	An understanding of professional and ethical responsibility.
**	g	An ability to communicate effectively.
	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
*	i	A recognition of the need for, and an ability to engage in life-long learning.
*	j	A knowledge of contemporary issues.
**	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Additional Notes or Comments

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Udated prereqs and exclusions to standard university format.

Crrected text title 3/30/12
Updated text edition, 4/4/13, CED

Update course goals, representative assignments, & grading. 4/18/14, GJV

Edited text info, 5/10/17, CED
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