# ECE 2060 (Proposed): Introduction to Digital Logic

## Course Description

Introduction to the theory and practice of combinational and clocked sequential networks.

**Transcript Abbreviation:** Int Digital Logic
**Grading Plan:** Letter Grade
**Course Deliveries:** Classroom, Greater or equal to 50% at a distance
**Course Levels:** Undergrad
**Student Ranks:** Sophomore
**Course Offerings:** Autumn, Spring
**Flex Scheduled Course:** Never
**Course Frequency:** Every Year
**Course Length:** 14 Week
**Credits:** 3.0
**Repeatable:** No
**Time Distribution:** 2.5 hr Lec, 1.0 hr Rec, 1.5 hr Lab
**Expected out-of-class hours per week:** 4.0
**Graded Component:** Lecture
**Credit by Examination:** No
**Admission Condition:** No
**Off Campus:** Never
**Campus Locations:** Columbus, Lima, Marion
**Prerequisites and Co-requisites:** Prereq: CSE 1222 (202), 2221 (221), Engr 1222 (EnGraph 167), 1281.01H (192.01H), or 1281.02H (192.02H); and Math 1152 (152), 1161.01 (161), 1161.02, 1172, or 1181H; and Physics 1250 (131), or 1260; and Engr 1182.01 (183), 1182.02, 1182.03, 1282.01H (193H), 1282.02H, 1282.03H, or 1186 (186), 1187 (187), and 1188 (185) concurrent, or 1187, 1188, and 1186 concurrent, or major in CIS or CIS-PRE; and CPHR 2.00 or above.
**Exclusions:** Not open to students with credit for 2000, 2000.02, 2000.07, 2001, 2010, or 2017.
**Cross-Listings:**

**Course Rationale:** Restructuring of Sophomore sequence. Splitting ECE2000 and ECE2100 into 3 courses.

**The course is required for this unit's degrees, majors, and/or minors:** Yes
**The course is a GEC:** No
**The course is an elective (for this or other units) or is a service course for other units:** Yes

**Subject/CIP Code:** 14.1001
**Subsidy Level:** Baccalaureate Course

## Programs

| Abbreviation | Description |
|---|---|
| CpE | Computer Engineering |
| EE | Electrical Engineering |

## General Information

There are actually seven 3 hour labs rather than fourteen 1.5 hour labs.
Lectures will meet three times per week for 45 minutes a session.

## Course Goals

| |
|---|
| Master the number representations used in today's digital systems and their arithmetic properties and conversion techniques |
| Master analyzing and synthesizing networks of combinatorial, digital logic elements |
| Be competent to analyze, design and synthesize digital clocked sequential circuits |
| Be familiar with modern computer tools for digital design, verification and simulation |
| Be familiar with how to implement their design schematics to hardware using modern FPGAs |
| Be competent in working in teams for lab experiments |
| Be familiar with digital circuit design methods |
| Be competent in reporting standards |
| Be competent in using laboratory instruments and laboratory methodology |
| Exposure to methodology for critical troubleshooting skills |

## Course Topics

| Topic | Lec | Rec | Lab | Cli | IS | Sem | FE | Wor |
|---|---|---|---|---|---|---|---|---|
| Number systems and conversion | 3.0 | | | | | | | |
| Boolean algebra | 2.0 | | | | | | | |
| Karnaugh maps | 2.0 | | | | | | | |
| Multi-level gate circuits | 2.0 | | | | | | | |
| Multiplexers, decoders and PLDs | 3.0 | | | | | | | |
| Latches and flip-flops | 3.0 | | | | | | | |
| Registers and counters | 3.0 | | | | | | | |
| Timing (delays, timing diagrams) | 2.0 | | | | | | | |
| Analysis of clocked sequential circuits (general models for sequential circuits, timing charts, state tables, graphs) | 4.0 | | | | | | | |
| Design of clocked sequential circuits | 4.0 | | | | | | | |
| Finite state machines, flow diagrams, mapping to flip-flop circuits with logic gates. | 4.0 | | | | | | | |
| Introduction to lab Equipment: Signal Generator and Oscilloscope, how to measure digital signals using the oscilloscope and the motivation for using digital signals | | | 3.0 | | | | | |
| Introduction to Quartus and the DE2 Board: HDL files, basic RTL components for simulation. Quartuss on-chip debugging tools, Signal Tap II and the In-System Memory Content Editor. | | | 6.0 | | | | | |
| Using the CODEC: Students are shown how to use the DE2s audio CODEC chip to perform conversions between analog and digital signals. | | | 3.0 | | | | | |
| Introduction to the Synthesizer: build a synthesizer, Students also learn how to use Matlab to create memory contents for ROM look-up tables. Finally students are introduced to bit shifting as a means of scaling signed and unsigned numbers. | | | 3.0 | | | | | |
| Electronic Keyboard: Students build a circuit that takes signals from PS2 keyboard and converts them into musical tones by applying the concepts and skills they have learned in the previous 5 labs. | | | 3.0 | | | | | |
| Demo Player Feature for an Electronic Keyboard: Students add an auto play feature to the electronic keyboard that automatically plays a short tune. Emphasizes the use of sequential components, testing of large Quartus project. | | | 3.0 | | | | | |

## Representative Assignments

| |
|---|
| Homework |
| Midterm Exams |
| Final Exam |
| Lab Reports |

## Grades

| Aspect | Percent |
|---|---|
| Homework | 15% |
| Midterm Exam 1 | 20% |
| Midterm Exam 2 | 20% |
| Final Exam | 25% |
| Lab Reports | 20% |

## Representative Textbooks and Other Course Materials

| Title | Author |
|---|---|
| *Fundamentals of Logic Design* | Roth, Jr. and Kinney |

## ABET-EAC Criterion 3 Outcomes

| Course Contribution | | College Outcome |
|---|---|---|
| *** | a | An ability to apply knowledge of mathematics, science, and engineering. |
| *** | b | An ability to design and conduct experiments, as well as to analyze and interpret data. |
| * | c | An ability to design a system, component, or process to meet desired needs. |
| ** | d | An ability to function on multi-disciplinary teams. |
| *** | e | An ability to identify, formulate, and solve engineering problems. |
| | f | An understanding of professional and ethical responsibility. |
| | g | An ability to communicate effectively. |
| | h | The broad education necessary to understand the impact of engineering solutions in a global and societal context. |
| | i | A recognition of the need for, and an ability to engage in life-long learning. |
| | j | A knowledge of contemporary issues. |
| *** | k | An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice. |

## Additional Notes or Comments

```
Initial Design: 9/10/14 Khan
Updated from 2.5 to 3 hr course 10/9/14

Synch prereqs and exclusiong to match university.  10/12/2015 BLA

Add recitations. Hours don't add up, but the in-person section takes the lecture with no
recitations and the on-line section has a recitation but no lecture. We need to have
recitations here or Carol can't schedule them. 10/12/2015

Edited text info 5/9/17, CED
```

**Prepared by:** Carol Duhigg