ECE 7020: Advanced Data Converters and Phase-Locked Loops

Course Description

A comprehensive overview of the most recent system architectures of data converters and phase-locked loops. Provides a good understanding how performance specifications and process technology limitations lead to implementation decisions. The presented principles are illustrated by examples and real life case studies.

Transcript Abbreviation: Data Conv & PLL
Grading Plan: Letter Grade
Course Deliveries: Classroom
Course Levels: Graduate
Student Ranks: Masters, Doctoral
Course Offerings: Autumn
Flex Scheduled Course: Never
Course Frequency: Even Years
Course Length: 14 Week
Credits: 3.0
Repeatable: No
Time Distribution: 3.0 hr Lec
Expected out-of-class hours per week: 6.0
Graded Component: Lecture
Credit by Examination: No
Admission Condition: No
Off Campus: Never
Campus Locations: Columbus
Prerequisites and Co-requisites: 5021 or 5023 or permission of instructor
Exclusions:
Cross-Listings:

Course Rationale: ADCs/PLLs are essential elements of electronic systems. The topics are not covered by any graduate course. It's a significant gap in our curriculum.

The course is required for this unit's degrees, majors, and/or minors: No
The course is a GEC: No
The course is an elective (for this or other units) or is a service course for other units: Yes

Subject/CIP Code: 14.1001
Subsidy Level: Doctoral Course

Course Goals

Learn various advanced mixed-signal integrated circuit design of data converters and phase locked loops.
Learn the specifications, performance metrics and tradeoffs of data converters and phase locked loops.
Learn the latest industrial trends and challenges pertaining to integration and semiconductor technologies.
Apply the acquired theoretical knowledge to perform design projects using IC PDKs and simulation and design tools.

Course Topics

Topic	Lec	Rec	Lab	Cli	IS	Sem	FE	Wor
Basic definitions, main tasks of data converters and/or phase locked loops and the challenges facing their implementation in VLSI applications	4.0							
Performance metrics, limitations, and tradeoffs	6.0							
System and circuit architectures and models	20.0							
Practical design considerations	4.5							
Implementation examples and product data sheets	4.5							

Representative Assignments

Homeworks
Quizzes
Exams
Design Projects

Grades

Aspect	Percent
Quizzes	20%
Exams	50%
Final Design Project	30%

Representative Textbooks and Other Course Materials

Title	Author
Class Notes	Vanessa Chen
Analog-to-Digital Conversion, ISBN 978-3319449715	Pelgrom, Marcel J.M.

ABET-EAC Criterion 3 Outcomes

Course Contribution		College Outcome
***	a	An ability to apply knowledge of mathematics, science, and engineering.
	b	An ability to design and conduct experiments, as well as to analyze and interpret data.
***	c	An ability to design a system, component, or process to meet desired needs.
	d	An ability to function on multi-disciplinary teams.
***	e	An ability to identify, formulate, and solve engineering problems.
	f	An understanding of professional and ethical responsibility.
	g	An ability to communicate effectively.
*	h	The broad education necessary to understand the impact of engineering solutions in a global and societal context.
	i	A recognition of the need for, and an ability to engage in life-long learning.
***	j	A knowledge of contemporary issues.
***	k	An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Additional Notes or Comments

5023 will cover basics of switch-capacitor circuits, data converters (flash and SAR ADCs, DACs) and PLLs. 7020 will cover advanced data converters, including pipeline, delta-sigma, time-interleaved and folding ADCs.

Change title and prefers 1/15/19 BLA

Prepared by: Vanessa Chen