Power Management for VLSI (Part I &II) – A short course

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Summary:

Developing power management solutions for VLSI systems and mixed-signal analog/RF System-on-Chip (SoC) requires engineers with solid background in both traditional power electronics design as well as analog/RF mixed-signal VLSI design. Power management circuits with such a VLSI and SoC focus are neither covered in graduate/undergraduate power electronics courses, nor in VLSI courses. With the growing demand in the semiconductor industry for expertise in this area, there is a serious shortage in formally-trained engineers who have the necessary background combination to design efficient and cost-effective solutions for such applications. This **two-part** course (each part is 3-days) introduces the principles of power management system and circuit design in VLSI systems. This includes: power delivery schemes and performance metrics/characterization of power converters; design principles of linear/switching power converters including linear and low-drop-out regulators, on-chip linear regulators, buck, boost, buck-boost, reconfigurable buck/boost, forward, and flyback switching power converters; loss mechanisms, modelling, and estimation in switching power converters; stability analysis, compensation techniques, and control schemes of linear/switching power converters; overview of practical implementations of buck converters; fully-integrated high-frequency buck converters with on-chip passives; multi-frequency single-inductor multiple-output (SIMO) switching power converters with on-chip outputs; high-current high-frequency multi-phase switching power converters; switching noise and EMI mitigation techniques in switching power converters and design considerations for mixed-signal/RF SoCs; linear/switching battery chargers. Part II includes design projects to exercise the knowledge acquired in an actual design. Attending part I before taking part II is recommended.

Learning Objectives (Part I):

Upon completing this part of the course, the participant will be able to:

- Understand power delivery schemes in VLSI systems.
- Understand power conversion/regulation system and circuit specifications and performance metrics.
- Understand circuit topologies, stability analysis, compensation techniques, control schemes, and design procedures of linear and low-dropout regulators and buck converters.
- Understand loss mechanisms, modelling, and estimation in switching power converters.
- Understand performance tradeoffs and the special requirements for large mixed-signal SoCs.

Learning Objectives (Part II):

Upon completing this part of the course, the participant will be able to:

- Understand the principles and operation of Boost, Buck-Boost, reconfigurable Buck/Boost, Forward, and Flyback switching power converters.
- Understand the principles and operation of high-frequency buck converters with on-chip passives, multi-frequency SIMO power converters with on-chip outputs, and high-frequency multi-phase high-current power converters.
- Develop a comprehensive understanding of switching noise and EMI mitigation techniques in switching power converters.
- Understand battery operation, charging algorithms, and linear/switching battery chargers.
- Perform a transistor-level design and simulation of a linear regulator and/or a buck converter.

Target Audience:
Analog and mixed-signal designers interested in understanding the principles of power management. Product, test, system, and application engineers involved with power management characterization and testing. Design engineers interested in power management in nanometer CMOS, and integration with mixed-signal SoCs. Researchers and graduate/undergraduate students interested in power management design. RFIC design engineers will find this course helpful in understanding issues related to powering RF circuits. Technical managers will also learn current technology limitations and future technology trends.

Outline (Part I):

Day One – System level concepts, performance metrics, linear regulators

Basic definitions, Power management tasks, Schemes and challenges in mixed-signal SoCs, Types of loads, Performance metrics of voltage regulators (power management language): DC, small-signal AC, and large-signal transient metrics, linear regulation concepts, linear and low-dropout regulator design, stability analysis and compensation.

Day Two – Linear and low-dropout regulators and Buck Converters

Continuation of linear and low-dropout regulator design; PMOS versus NMOS power FETs; on-chip linear and low-dropout regulators; switching power conversion concepts; buck switching regulators, steady-state operation/equations, continuous/discontinuous conduction modes, loss mechanisms modeling and estimation, load-based control techniques (pulse width and pulse frequency modulation).

Day Three – Buck Converters modeling and control

AC and small-signal modeling of buck regulators; voltage-mode controllers and compensation (type-I, type-II, and type-III); current-mode controllers and compensation (slope compensation); hysteretic and PFM controllers and compensation (emulated ripple control); gated-oscillator and burst-mode control, practical implementation examples.

Outline (Part II):

Day One – Other inductor-based switching regulators
Boost, Buck-Boost, reconfigurable Buck/Boost, Forward, and Flyback steady-state operation/equations, continuous/discontinuous conduction modes, small-signal modeling and stability; fully-integrated high-frequency buck converters with on-chip passives; multi-frequency single-inductor multiple-output (SIMO) power converters with on-chip outputs; high-current multi-phase switching power converters.

Day Two – Switching noise and EMI mitigation techniques and battery chargers

Impact of switching noise and EMI on SoC performance, mitigation techniques including active ripple cancellation, multi-phase converters, delta-sigma control, snubber circuits, frequency hopping/stepping, and spur-free switching; battery Chargers, types of batteries, charging profiles, constant-current constant-voltage charging, pulse charging, linear and switching battery charger topologies, multi-cell battery chargers, battery monitoring circuits and fuel gauging.

Day Three – Design Projects

Two transistor-level design projects will be assigned to implement and simulate in a standard CMOS technology under the supervision of the instructor. The default projects are a buck converter and a low-dropout regulator, but other converter types are available. Detailed design procedure/steps will be provided as part of the course notes. Participants must have access (through VNC or a similar tool) to a Linux workstation with a Cadence toolset and a PDK of a CMOS technology through their employer. Participants should set up a Cadence database/library ahead of the project day. Participants not interested in transistor-level design are not required to attend the project day, but will find it useful to attend as discussions will offer additional insights into the theoretical material from prior days.

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POWER MANAGEMENT RESEARCH LAB

Ayman Fayed received his B.Sc. degree in Electronics & Communications Engineering from Cairo University in 1998, and his M.Sc. and Ph.D. degrees in Electrical & Computer Engineering from The Ohio State University in 2000 and 2004, respectively. From 2000 to 2009, he held several technical positions in the area of analog and mixed-signal design at Texas Instruments Inc., where he contributed to many product lines for wire-line, wireless, and multi-media devices. From 2000 to 2005, he was with the Connectivity Solutions Dept. at TI, where he worked on the analog frontend design of high-speed wire-line transceivers such as USB, IEEE1394b, and HDMI, and on fully integrated switching/linear regulators and battery chargers for portable media players. From 2005 to 2009, he was a member of the technical staff with the wireless analog technology center at TI, where he worked on delta-sigma data converters for various wireless standards, and on the development of fully-integrated power management solutions for mixed-signal SoCs with multi-RF cores in nanometer CMOS. Dr. Fayed joined the Dept. of Electrical & Computer Engineering at Iowa State University in 2009, where he held the Northrop Grumman Assistant Professorship. He then joined the Dept. of Electrical & Computer Engineering at The Ohio State University in 2015, where he is currently a professor. He is the founder and director of the Power Management Research Lab (PMRL) and his current research interests include on-chip power supplies for dynamic energy distribution in VLSI systems, high-frequency switching regulators with on-chip and on-package passives for SoCs, low-noise power supplies and power supply modulators for analog and RF circuits, energy-harvesting circuits for power-restricted & remotely-deployed devices/systems, and analog/mixed-signal and power converter design in SiC and GaN technologies. He is currently an associate editor for IEEE TCAS-I and previously for TCAS-II, and serves in the technical program committee of RFIC, ISCAS, APEC, and the steering committee of MWSCAS. He is the author/co-author of many publications in the field and holds 8 US patents. Dr. Fayed is a recipient of NSF CAREER Award in 2013, and a co-recipient of the 2015 Darlington Best Transactions Paper Award from the IEEE Circuits and System Society. Dr. Fayed is a senior member of IEEE.

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