SYLLABUS ECE 5020: Mixed Signal VLSI

Autumn 2019

Description: Design and circuit analysis of basic VLSI structures such as registers, cell libraries, memory, digital and analog I/O. Students will be introduced to schematic capture, simulations, timing analysis and physical layout using cadence design tools. There will be an emphasis on CMOS circuit design, culminating in a design project.

Learning Goals:

1. Be familiar with integrated circuit design flows and project planning.
2. Be competent in CMOS circuit performance characterization using CAD tools.
3. Master the analysis and design of CMOS logic circuits
4. Be competent in clean physical layout of standard CMOS logic cells using CAD tools.
5. Be competent in analysis and design of arithmetic logic building blocks and memory.
6. Be exposed to system design, including interconnect, clocking and power distribution.
7. Be competent in working effectively in a team to complete a design project.

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Text: Required: *Digital Integrated Circuits, 2nd Edition*, Rabeay, Chandrakasan, Nikolic, Prentice Hall, 2003.

References (supplemental reading): *CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition*, by N. Weste and D. Harris, Addison-Wesley, 2011.

Topics Covered:
Introduction
MOS Transistor
The CMOS inverter
Combinational logic structures
Sequential logic gates
Design methodologies
Interconnect: R, L and C
Timing Analysis
Arithmetic building blocks
Memory and array structures