SYLLABUS ECE 7023: HIGH-SPEED INTERFACE CIRCUITS AND SYSTEMS

Spring 2020

Description: Analysis and design of link architectures and circuits for wireline communication systems. Emphasis on design intuition, link budgeting and power/performance trade-offs in implementation of data links in advanced CMOS process. Topics include channel characterization, noise analysis, equalization, transmitter and receiver circuits, signaling schemes, clocking, synchronization and timing recovery circuits.

Learning Goals:

1. Learn fundamentals of high-speed data link design
2. Learn system architecture using modeling tools
3. Understand the challenges of designing high-speed wireline circuits through a design project using advanced CMOS.
4. Be exposed to several link standards, including USB-Type C, Thunderbolt, PCIe and DDR.

Instructor:

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Text:

No text book needed. *Lecture Notes, IEEE Journal Papers (JSSC, TCAS) and Conference Proceedings (ISSCC, VLSIC, CICC)*

References (supplemental reading):

Digital Systems Engineering, W. Dally and J. Poulton, Cambridge University Press, 1998

Topics Covered:

Introduction to high-speed links
Channel characterization
Noise and jitter
Equalization
Signaling schemes
Transmitter circuit design
Receiver circuit design
Different clocking schemes
Timing recovery
Power and Clock Distribution