CMOS technology standard library cell. The estimated equivalent gate counts for the three methods are summarised in Table 1. As listed in Table 1, the proposed TS-BDI method reduces hardware complexity in the 64-channel digital receive beamformer by around 36.0% over the case of the CON method. Compared to the TS-LDI, the TS-BDI method slightly increases the hardware complexity, i.e. by around 3.2%, while improving the SNR.

Conclusion: A new focusing delay calculation method based on time-sharing bilinear delay interpolation is proposed to reduce hardware complexity while maintaining the comparable image quality for portable ultrasound systems. The proposed TS-BDI method shows improvement in SNR compared to the TS-LDI in the simulation study. In addition, it substantially decreases the hardware complexity in the digital dynamic receive beamformer. We believe that the proposed method could be used for further miniaturising portable ultrasound systems while maintaining image quality.

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One or more of the Figures in this Letter are available in colour online.

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Correlated level shifting integrator with reduced sensitivity to amplifier gain

T. Musah and U.-K. Moon

An integrator that achieves gain enhancement by utilising correlated level shifting is proposed. The integrator realisation avoids the use of an extra settling phase usually required in correlated level shifting. The superior performance of the proposed integrator compared to the conventional integrator is shown via simulation results.

Introduction: Op-amp gain sensitivity in integrators is known to be the limiting factor for accuracy in delta-sigma modulators. This limitation is more severe when cascaded modulator topologies are used owing to mismatch between analogue and digital transfer functions. Several techniques, including correlated double sampling (CDS), have been proposed to alleviate the op-amp gain sensitivity. However, these techniques either require an extra phase for proper operation or increase the sampled thermal noise. Correlated level shifting (CLS) [1] offers a possible way to achieve gain enhancement without added thermal noise. Direct application of CLS in an integrator results in a three-phase realisation. A CLS integrator that uses only two phases for operation is proposed. The scheme utilises the memory of integrators to predict the estimate of the output signal, thus skipping the phase devoted to estimation.

Correlated level shifting integrator: The schematic diagram in Fig. 1 shows a conventional switched-capacitor integrator. The DAC signal is not shown for simplicity. The input signal is sampled at the end of ϕ_1 and transferred to the feedback capacitor during ϕ_2. The output voltage is sampled at the end of ϕ_1 to realise a full delay integrator. The transfer function of the integrator, given an op-amp DC gain of A, can be written as

$$\frac{V_O}{V_S} = \left(\frac{C_s}{C_f}\right)\left[\frac{(1-\delta)z^{-1}}{1-(1-\alpha)z^{-1}}\right]$$

where

$$\delta = \frac{1}{1+A\beta}; \quad \alpha = \frac{1-\beta}{1+A\beta}; \quad \text{and} \quad \beta = \frac{C_f}{C_s + C_f}$$

To minimise the magnitude error (δ) and phase error (α) in the transfer function, the op-amp gain has to be as large as possible. The CLS technique provides a simple power-efficient way of increasing the effective loop gain, but a three-phase operation is necessary to implement the current realisation. One phase is allotted for sampling the input, another to charge an estimate of the output voltage on a capacitor and the final phase to level shift the op-amp output using the capacitor.
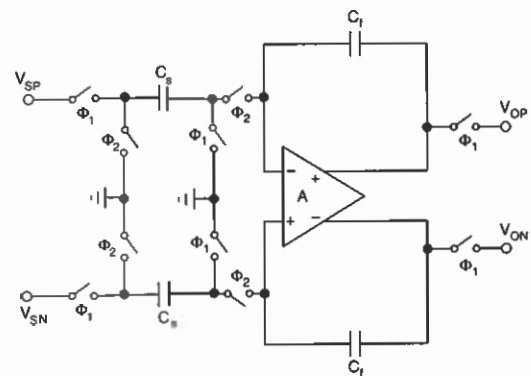

Fig. 1 *Conventional integrator*

In an integrator, the phase error is more detrimental than the magnitude error and determines the gain at low frequencies. If instead of estimating the current integrator output, we use the previous integrator output for level shifting, we avoid the extra phase required for estimation. This allows a two-phase realisation of the CLS integrator. While this may increase the amplifier swing compared to regular CLS, the error at the op-amp virtual ground will depend only on the current input. Fig. 2 shows the proposed CLS integrator. The operation is similar to that of the conventional integrator with an additional switched-capacitor network at the output to implement the level shifting. As the next stage's sampling capacitors sample the output during ϕ_1, the level shifting capacitors (C_{LS}) also sample the output voltage. The C_{LS} capacitors are then used to level shift the output of the op-amp during the charge transfer phase, ϕ_2. If the voltage sampled across C_{LS} at the end of ϕ_1 matches the previous output voltage, then the settling error at the virtual ground will be due to only the new charge, driving the phase error (α) to zero. However, the voltage sampled on C_{LS} is less than the output at the end of ϕ_2 owing to the finite loop gain in the hold phase (ϕ_1). As a result, the magnitude phase errors are suppressed by the loop gain during ϕ_1 at low frequencies, yielding

$$\delta = \frac{1}{1+A\beta(1+A)} \text{ and } \alpha = \frac{1-\beta}{1+A\beta(1+A)}$$

The swing at the output of the op-amp will depend on the ratio of the level shifting capacitance to the total capacitance at the output. The larger the level shifting capacitor, the lower the swing but the higher the op-amp power consumption. Thus, there is a trade-off between the op-amp swing requirement and power consumption when choosing C_{LS}.

Comparison with correlated double sampling: The CLS integrator does not remove offset, unlike the CDS integrator of [2]. However, the proposed CLS integrator does not suffer from the increased thermal noise prevalent in CDS integrators. Moreover, while the achieved gain enhancement is similar in the two techniques, the CLS integrator has the possibility for better gain if cross-coupling [3] is used to improve

the matching between the previous output signal and what gets used for level shifting the op-amp output.
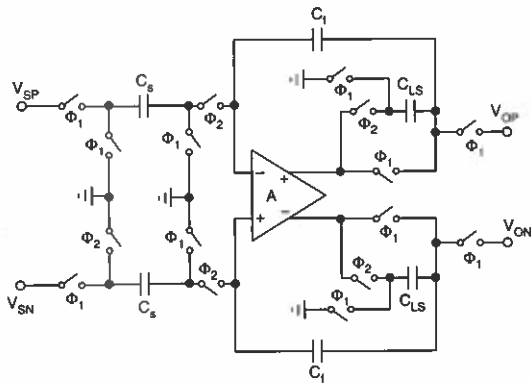

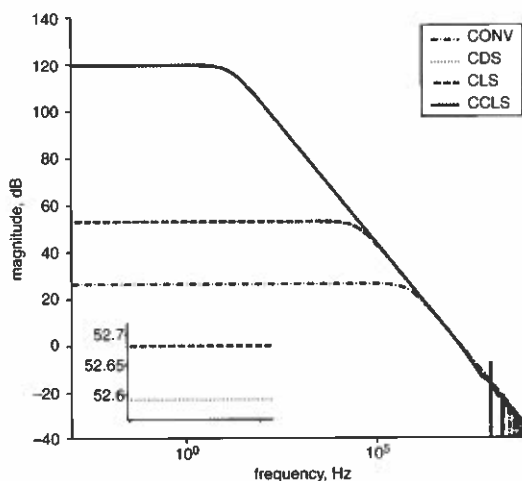**Fig. 2** *Correlated level shifting integrator*

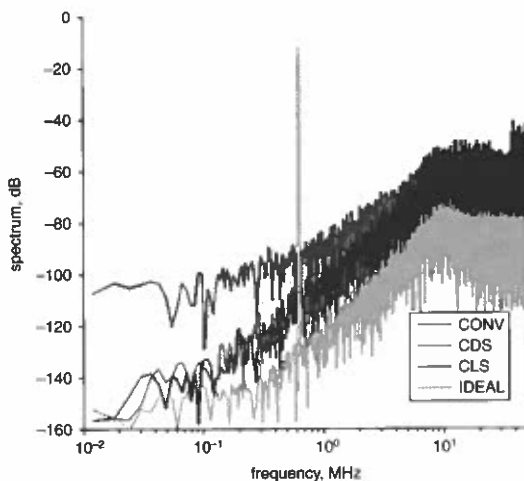**Fig. 3** *Simulated frequency response of integrators*

Fig. 4 *Simulated output spectra of modulators*

Simulation results: The transfer functions of the conventional integrator of Fig. 1, the CDS integrator of [2] and the proposed CLS integrator of Fig. 2 were simulated in Spectre using PAC analysis. The DC gain of the op-amp was chosen to be 26 dB and the capacitors were chosen such that $C_s = C_f = C_{LS}$, where C_s is 100fF. As can be seen from Fig. 3, the conventional integrator has a low frequency gain of 26 dB, while the CDS and CLS integrators obtain a low-frequency gain of 52 dB (double that of the conventional). The transfer function of the CLS integrator with a cross-coupled gain enhancement capacitor (CCLS) is also shown for completeness, but as discussed in [3], it is sensitive to op-amp gain, making it difficult to achieve very high low-frequency gain in practice, so no further discussion of it is included.

The integrators were also used to design 2-0 MASH modulators. The first stage is a second-order CIFB structure with a binary quantiser. The second stage is an 8 bit flash. The op-amp DC gain was maintained at 26 dB while the two integrators in the loop were designed to have a closed-loop gain of 0.5 V/V each. Simulation results from Spectre in Fig. 4 show that the modulator with the conventional integrator suffers the worst noise leakage. It achieves an SQNR of 64.0 dB at an OSR of 64 while the modulators with the CDS and CLS integrators achieve an SQNR of 80.7 and 82.0 dB, respectively. The conventional integrator with an op-amp gain of 120 dB (representing ideal) achieves an SQNR of 102.3 dB and it is included in Fig. 4 as a reference. The difference in SQNR between the ideal and the proposed technique is because the effective low-frequency gain is 56 dB in the proposed integrator, 64 dB below the ideal integrator's low-frequency gain.

Conclusion: An integrator that employs the CLS technique to improve its phase error is proposed. The integrator operation is completed in only two phases owing to the leveraging of the integrator memory. Simulation results show similar gain enhancement to CDS, but without the additional thermal noise. The integrator also offers the possibility for further gain improvement.

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Mixed-mode QPSK demodulator for home networking applications

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A mixed-mode QPSK demodulator for home networking application is demonstrated. The target application is high-bandwidth data transmission through the CATV line at home. A prototype chip realised by a 0.18 μm CMOS process can demodulate 1 Gbit/s QPSK data with 1.7 GHz carrier frequency in a 20 m CATV line link. It consumes 20.8 mW from an 1.8 V power supply while the area is 170 × 200 μm².

Introduction: There is growing interest in realising high-speed mixed-mode demodulators for various home networking applications. Although digital demodulators are widely in use, the increase in data rate makes designing ADCs challenging. Many home networking applications require Gbit/s data transmission rate, and ADCs having GSymbol/s sampling rate can consume lots of power and chip area. We have previously demonstrated the mixed-mode binary-phase-shift keying (BPSK) demodulation scheme, which does not require an ADC [1, 2]. We showed that slicing BPSK signals with a hard limiter produces signal shapes very similar to a baseband NRZ data sequence and, consequently, a mixed-mode clock and data recovery (CDR) structure can be successfully applied for demodulation of BPSK signals.

This Letter demonstrates the extension of our previous work into mixed-mode quadrature-phase-shift keying (QPSK) demodulation. We