

# Correlated level shifting technique with cross-coupled gain-enhancement capacitors

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A new technique is proposed to compensate for the loop gain degradation in correlated level shifting. The technique allows the use of a simple single-stage opamp with low gain to realise high effective loop gain. The effect of gain variations on the performance of the proposed correlated level shifting technique is discussed.

**Introduction:** The scaling of process technology has enabled the design of low-power, high-speed digital signal processing blocks. However, analogue circuits have seen reductions in both intrinsic gain and available swing. The correlated double sampling (CDS) technique proposed in [1] provides gain enhancement at the cost of noise power and speed. A parallel correlated double sampling (PCDS) technique presented later in [2] avoids the noise power penalty of CDS. However, both techniques do not allow for high signal swing since they are limited by headroom considerations. The correlated level shifting (CLS) [3] technique offers a solution to both the gain and the swing limitation. However, a level shifting capacitor, used to maintain the opamp output swing low, causes a reduction in loop gain. The proposed CLS scheme employs cross-coupling capacitors to greatly enhance the effective loop gain in the presence of the level-shifting capacitor.

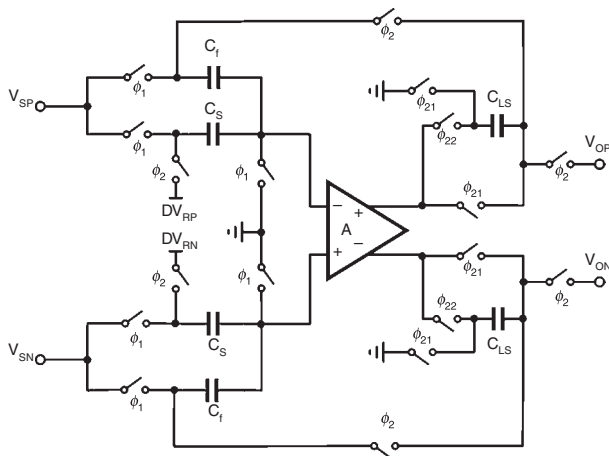


Fig. 1 Correlated level shifting MDAC

**Improved correlated level shifting technique:** Fig. 1 shows a realisation of the CLS technique in a multiplying digital-to-analogue converter (MDAC). The MDAC is configured for a 1.5 bit pipeline stage. The input signal ( $V_S$ ) is sampled onto  $C_S$  and  $C_f$  during  $\phi_1$ . The amplification phase,  $\phi_2$ , is split into two phases:  $\phi_{21}$  for estimation and  $\phi_{22}$  for level shifting and amplification. The level shift capacitor  $C_{LS}$  samples the estimated output voltage at the end of  $\phi_{21}$ , and is placed in series with the opamp output during  $\phi_{22}$ . This brings the opamp output back to the common-mode voltage, forcing a more accurate virtual ground. During  $\phi_{22}$ , there is charge sharing between  $C_{LS}$  and the total load capacitance ( $C_{LD}$ ). This degrades the loop gain and causes a nonzero swing at the opamp output in  $\phi_{22}$ . The smaller the capacitance of  $C_{LS}$ , the worse the loop gain and the larger the opamp output swing in  $\phi_{22}$ . The output voltage at the end of  $\phi_{22}$  is

$$V_o = \left( \frac{C_s + C_f}{C_f} \right) \left[ 1 - \frac{1 + \lambda}{(1 + A_{21}\beta)(1 + A_{22}\beta + \lambda)} \right] V_S$$

where

$$\beta = \frac{C_f}{C_s + C_f}, \quad \lambda = \frac{C_{LD}}{C_{LS}}$$

The change in the opamp DC gain from high swing operation in  $\phi_{21}$  to low swing operation in  $\phi_{22}$  is captured in the gain parameters  $A_{21}$  and  $A_{22}$ . For an infinitely large  $C_{LS}$ ,  $\lambda$  is zero and the effective loop gain is a product of the loop gains in  $\phi_{21}$  and  $\phi_{22}$ . A realistic design with  $C_{LS} = C_{LD}$  yields  $\lambda = 1$  and about 6 dB loss in effective loop gain. However, this implies doubling the total load capacitance during  $\phi_{21}$ ,

thus increasing the power or reducing the speed of the MDAC. The charge sharing between  $C_{LS}$  and  $C_{LD}$  could be reduced if a two-stage opamp is used [3]. This is because the compensation capacitor provides some of the charge needed at the output. However, a two-stage opamp is not always desired for low power submicron realisations and the value of the compensation capacitor is determined by phase margin requirements.

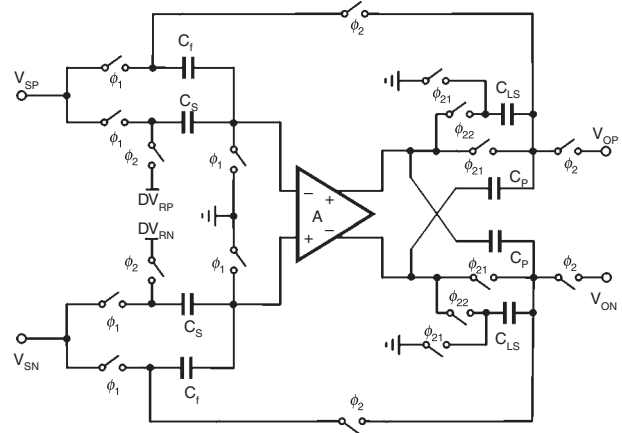


Fig. 2 Correlated level shifting MDAC with improved gain

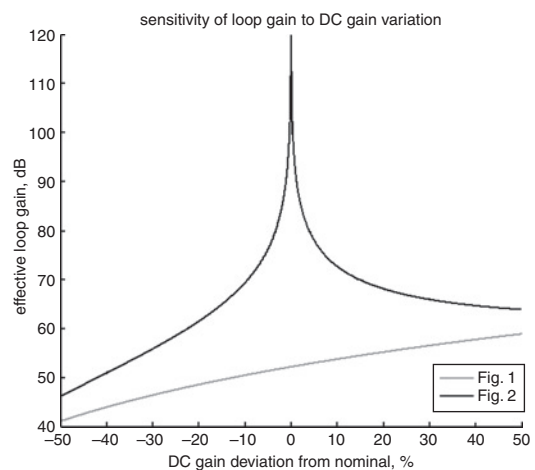


Fig. 3 Effect of DC gain variation on effective loop gain

A CLS MDAC that uses a single-stage opamp and does not suffer from loop gain degradation is shown in Fig. 2. At the end of  $\phi_{21}$ , while the output voltage is sampled on  $C_{LS}$ , the differential output voltage is held across  $C_P$ . The extra charge needed at the output for a more accurate virtual ground is provided through  $C_P$  and  $C_{LS}$ . Proper sizing of  $C_P$  allows its use to provide all the charge needed at the output. All the charge injected into (drawn from)  $C_P$  is drawn from (injected into)  $C_{LD}$ . The output voltage at the end of  $\phi_{22}$  now becomes

$$V_o = \left( \frac{C_s + C_f}{C_f} \right) \left[ 1 - \frac{1 + \lambda}{(1 + A_{21}\beta)(1 + A_{22}\beta + \lambda)} \right] V_S$$

where

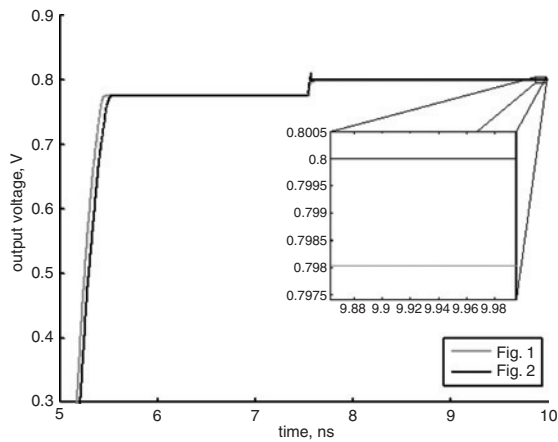
$$\lambda = \frac{C_{LD} - C_P(A_{21}\beta - 1)}{C_{LS}}$$

It is obvious from the above expression that designing for  $\lambda = -1$  will result in an MDAC with no gain error (infinite effective loop gain). Since the value  $\lambda$  is dependent on the opamp DC gain in  $\phi_{21}$ , the designer will need to precisely know the value of  $A_{21}$  to accurately choose  $C_P$ . The sensitivity of the effective loop gain to DC gain deviations from its nominal value due to process and device mismatch is shown in Fig. 3. For the plot, we used an open loop DC gain of 36 dB and assumed it does not change between  $\phi_{21}$  and  $\phi_{22}$ . Also,  $C_{LD} = 800$  fF,  $C_{LS} = 440$  fF and  $C_P = 40$  fF. The effective loop gain of the proposed CLS MDAC of Fig. 2 is at least doubled (in dB) as long as the gain deviation from the nominal is less than 20%. This

range will be further widened when the higher  $A_{22}$  is factored into the effective loop gain plot. Although the effective loop gain of the original CLS MDAC of Fig. 1 is less sensitive to DC gain deviations, it remains lower than that of Fig. 2 for any DC gain value.

**Offset and noise performance:** There is an additional  $kT/C$  noise power added by the level shifting network. However, since the network is at the output of the MDAC, any noise from it is attenuated by the loop gain. Therefore, the extra noise due to the level shifting network is not significant. However, offset is not attenuated and it sees the same gain to the output as the input signal. The offset and flicker noise could be compensated for by other design techniques for narrowband applications where they limit performance.

**Simulation results:** Simulations were run to compare the settling accuracy of the improved CLS MDAC of Fig. 2 with the CLS MDAC of Fig. 1 using identical opamps with 36 dB open loop DC gain. The same capacitance values were used in both MDACs and  $C_p$ , 40 fF. The result is shown in Fig. 4 for the amplification phase,  $\phi_2$ , when a 100 MHz clock is used. The jump at the beginning of  $\phi_{22}$  is due to injection of the corrective charge at the output by  $C_p$ . The height of the jump depends on the size of the load capacitance compared to the output capacitance [3]. As expected, the settling accuracy at the end of  $\phi_{21}$  (7.5 ns) is the same for both circuits, and corresponds to a loop gain of 30 dB. Also, the CLS MDAC of Fig. 1 settles slightly faster in  $\phi_{21}$  because the total load capacitance is less. However, the improved CLS MDAC of Fig. 2 achieves higher than 100 dB effective loop gain while the CLS MDAC of Fig. 1 achieves 52 dB effective loop gain at the end of  $\phi_2$ .



**Fig. 4** Simulated settling response of proposed CLS MDAC to 400 mV input step (800 mV ideal output)

**Conclusion:** An improved correlated level shifting technique has been proposed. It avoids charge sharing between the level shifting capacitor and the capacitance at the output, hence enhancing the loop gain. The technique has been presented using an MDAC for pipeline/algorithmic ADCs, but is applicable to any other switch capacitor applications such as integrators and biquads.

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